URN etd-0407109-183703-181
Author Sung-Min Lin
Author's Email Address No Public.
Statistics This thesis had been viewed 44 times. Download 0 times.
Department
Year 2005
Semester 1
Degree Master
Type of Document Master's Thesis
Language English
Title A Platform for High-Level Synthesis and Post-Simulation of Self-Timed Systems
Date of Defense 0000-00-00
Page Count 105

Keyword
high-level synthesis
asynchronous circuit
HDL
extended-burst mode
channel level
handshaking level

Abstract
We propose an asynchronous platform which allows FPGA board docking onto an Arm-based development kit to simulate and verify the VHDL-compatible coding styles in the synthesis. This high-level synthesis targets on the self-timed circuit implementation technique since asynchronous design is gradually adapted to the circuit engineering alternatives. The self-timed system design methodology lacks of complete tool set to cover the entire engineering design processes; therefore, varieties of applicable software are created and left un-integrated. We set up a design flow to stricken the asynchronous design methodology by reducing the complexity of transforming channel-level to handshaking-level in the high-level synthesis and simulation.

The feasibility of a successful asynchronous design methodology depends on completeness of series of software simulations and hardware verification. Thus, we impose a rigid guideline for VHDL programming on conversion of channel package to 4-phase handshaking protocol and later separate the programmed design into controller and datapath by syntax property. Further to the translation of the program, we use 3D plus timing information modeling and tools for datapath optimization in the final synthesis. In the end, the design verification will be downloaded to FPGA for circuit simulation, and the test patterns or the testbench will be loaded to the development kit or the platform we have established in order to compare the actual result with our desired signal patterns on the platform.
Advisory Committee Jung-Lin Yang - advisor

Files No Any Full Text File.
Date of Submission 2006-08-02